IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application:
Application No.:
Filed:
Title:

Commissioner for patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST (REVOCATION OF PRIOR POWERS)

As assignee of record of each of the patent applications listed in the table of **Attachment** A,

REVOCATION OF PRIOR POWERS OF ATTORNEY

all powers of attorney previously given in each of the listed patent applications are hereby revoked, and

NEW POWER OF ATTORNEY

the following attorneys/agents are hereby appointed to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: I hereby appoint all attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as the attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence about the application be addressed to the address filed under the same USPTO Customer Number.

000047390
Patent Trademark Office

Please direct all future correspondence and telephone calls to:

Daniel R. McClure, Reg. No. 38,962
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

ASSIGNEE OF ENTIRE INTEREST

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ASSIGNEE CERTIFICATION

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with **Taiwan Semiconductor Manufacturing Co., Ltd**, I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

Date: 2/6/2012

Keith A. Chanreo
Director of Intellectual Property Division

Attachment A

No.	Filing No.	Filing Date	Title	Assignment (Reel/ Frame)
1	08/893,642	07/11/1997	Semiconductor memory with a novel column decoder for selecting a redundant array	008635/0183
2	08/738,214	10/25/1996	Integrated circuit output driver incorporating power distribution noise suppression circuitry	008285/0279
3	08/892,216	07/14/1997	RC delay circuit for integrated circuits	008644/0232
4	08/944,771	10/06/1997	Local word line decoder for memory with 2 1/2 MOS devices	008758/0137
5	08/944,571	10/06/1997	Local word line decoder for memory with 2 MOS devices	008754/0693
6	08/893,641	07/11/1997	Bandgap reference circuit	008635/0216
7	08/891,973	07/11/1997	Adjustable, full CMOS input buffer for TTL, CMOS, or low swing input protocols	008644/0688
8	09/498,982	02/07/2000	Adjustable, full CMOS input buffer for TTL, CMOS, or low swing input protocols	008644/0688 as in the Parent Paten 6023174
9	09/030,197	02/25/1998	Multiple-bit, current mode data bus	009045/0700
10	09/709,590	11/13/2000	Multiple-bit, current mode data bus	009045/0700 as in the Parent Patent 6184714
11	09/709,598	11/13/2000	Multiple-bit, current mode data bus	009045/0700 as in the Parent Patent 6184714
12	09/189,439	11/10/1998	Method and apparatus of an output buffer for controlling the ground bounce of a semiconductor device	009575/0573
13	09/292,660	04/15/1999	Any value, temperature independent, voltage reference utilizing band gap voltage reference and cascode current mirror circuits	009914/0257
14	09/085,613	05/27/1998	Schmitt trigger input stage	009208/0959

15	09/177,341	10/23/1998	Method to test auto-refresh and self refresh circuitry	009542/0733
16	09/085,332	05/26/1998	Antifuse programming and detecting circuit	009209/0850
17	09/075,745	05/11/1998	EPROM used as a voltage monitor for semiconductor burn-in	009179/0643
18	09/633,645	08/07/2000	Bias monitor for semiconductor burn-in	009179/0643 as in the Parent Patent 6137301
19	09/876,595	06/08/2001	EPROM used as a voltage monitor for semiconductor burn-in	009179/0643 as in the Parent Patent 6262588
20	09/047,541	03/25/1998	Clock synchronized delay scheme using edge-triggered delay lines and latches with one clock lock time	009109/0012
21	09/080,115	05/18/1998	Electrically programmable fuse	009203/0268
22	09/621,373	07/21/2000	Electrically programmable fuse	009203/0268 as in the Parent Patent 6100746
23	09/621,374	07/21/2000	Electrically programmable fuse	009203/0268 as in the Parent Patent 6100746
24	09/120,360	07/22/1998	Bias scheme to reduce burn-in test time for semiconductor memory while preventing junction breakdown	009343/0608
25	09/063,997	04/21/1998	Apparatus for generating a timing signal	009142/0740
26	09/047,540	03/25/1998	Edge triggered delay line, a multiple adjustable delay line circuit, and an application of same	009117/0252
27	09/358,013	07/21/1999	Device and method for generating a variable duty cycle clock	010124/0590
28	09/222,271	12/28/1998	Enhanced random number generator	009691/0907
29	09/400,353	09/20/1999	Low power high-speed bus receiver	010267/0193
30	09/429,402	10/28/1999	Semiconductor memory device with function of equalizing voltage of dataline pair	010353/0593

31	09/429,595	10/28/1999	Dynamic precharge redundant circuit for semiconductor memory device	010353/0816
32	09/548,032	04/12/2000	Redundant decoder having fuse-controlled transistor	010739/0372
33	09/422,022	10/20/1999	Layout for pull-up/pull-down devices of off-chip driver	010336/0138
34	11/636,524	12/11/2006	Static random access memory	018699/0617
35	08/958,205	10/17/1997	Semiconductor memory device with improved read signal generation of data lines and assisted precharge to mid-level	008865/0698
36	08/995,379	12/22/1997	High-speed synchronous write control scheme	008937/0059
37	09/044,198	03/17/1998	Multiple input/output level interface input receiver	009067/0149
38	09/044,205	03/17/1998	Input receiver for limiting current during reliability screening	009067/0105
39	09/036,726	03/06/1998	Crow-bar current reduction circuit	009070/0464
40	09/046,408	03/23/1998	Regulator system for an on-chip supply voltage generator	009106/0174
41	09/135,252	08/17/1998	Multiple data clock activation with programmable delay for use in multiple CAS latency memory devices	009402/0054
42	09/071,601	05/01/1998	Timing circuit that selectively triggers on a rising or falling input signal edge	009159/0838
43	09/064,884	04/20/1998	Dynamically adjustable on-chip supply voltage generation	009132/0385
44	09/103,676	06/23/1998	Distributed array activation arrangement	009278/0479
45	09/266,006	03/12/1999	On-chip-generated supply voltage regulator with power-up mode	009819/0532 010067/0141
46	09/056,546	04/07/1998	Method and circuit for disabling a two-phase charge pump	009119/0624
47	09/156,183	09/17/1998	Mock wordline scheme for timing control	009491/0919

48	09/320,427	05/26/1999	Timing circuit for a burst-mode address counter	010163/0925 010375/0650
49	09/262,503	03/04/1999	Internal charge pump voltage limit control	009814/0357 010069/0591
50	09/274,211	03/23/1999	Switch level simulation with cross-coupled devices	009865/0295 010186/0719
51	09/498,985	02/07/2000	Self-refresh test time reduction scheme	010598/0451
52	09/747,233	12/26/2000	Test mode for verification of on-chip generated row addresses	011429/0905
53	09/764,243	01/19/2001	Reticle option detection circuit	011492/0426
54	09/670,405	09/28/2000	Local bit switch decode circuit and method	011166/0331
55	09/640,533	08/17/2000	Clock duty cycle correction circuit	011147/0395
56	09/802,458	03/09/2001	Method of buffer management and task scheduling for two-dimensional data transforming	011611/0234
57	11/480,378	07/05/2006	Multiphase Multistage Single Frequency Charge Pump	018042/0016
58	11/833,160	08/02/2007	Voltage Regulator	019651/0118
59	08/968,155	11/17/1997	Method of forming a new bipolar/CMOS pixel for high resolution imagers	008824/0891
60	09/053,854	04/02/1998	Operation methods for active BiCMOS pixel for electronic shutter and image-lag elimination	009125/0212
61	09/886,776	06/21/2001	Method and apparatus of controlling a pixel reset level for reducing an image lag in a CMOS sensor	011938/0574
62	09/896,486	06/29/2001	On-chip design-for-testing structure for CMOS APS (active pixel sensor) image sensor	012155/0264
63	09/896,426	06/29/2001	Pixel defect correction in a CMOS active pixel image sensor	017648/0115
64	09/671,565	09/27/2000	Method of bad pixel correction	011188/0112

65	09/670,685	09/27/2000	Method and apparatus for dark level intergration of image sensor without integrating bad pixels	011142/0503
66	09/671,566	09/27/2000	Method of defective pixel address detection for image sensors having windowing function	011186/0175
67	09/671,567	09/27/2000	Method of defective pixel address detection for image sensors	011186/0205